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TECHNICAL SUMMARY REPORT

ON

Design, Development and Delivery on One (1) Breadboard Model and Three (3) Production Units of a 75 VA Integrated Static Inverter

(27 April 1965 to 27 May 1965)

Contract No. NAS8-11925

11 June 1965

Prepared for

National Aeronautics and Space Administration

George C. Marshall Space Flight Center

Huntsville, Alabama

[redacted]

TECHNICAL DISCUSSION

A. Progress Report for Month of May, 1965

1. Power Supply System

A discrete component breadboard version of the inverter and output filter portion of the power supply has been built and tested for various loading conditions. A variable dc lab supply and a pulse generator were used to simulate the dc regulator and oscillator/countdown circuit, respectively.

The Johnson counter has been built with SN530 flip flops.

The breadboard model was built with discrete Darlington power transistors instead of a single power transistor and integrated circuit driver after efficiency calculations indicated this was the best approach.

Work has also begun on the regulator. From efficiency considerations a "switching" regulator is deemed necessary. One approach is in block diagram form and a second straightforward technique is presently being breadboarded.

Tentative specifications have been submitted to the device design engineers on the power switches and the integrated counters. Oscillator specifications have been forwarded to two manufacturers of temperature compensated crystal oscillators. Three suppliers (two outside and one in-house) have been contacted on system packaging of the three production units.

The inverter breadboard was tested with 0, 10%, 100% and 150% rated output with resistive loads and also ~ 150% rated output at 50% lagging power factor. Preliminary data indicates satisfactory operation in all instances.

2. Progress Report on Subsections

a. Circuit Design

The breadboard circuit as it now exists is shown in Figures 1A and 1B. The dc power is supplied to the power switches from a dc lab supply. Also, the timing pulses are obtained from a pulse generator and the Johnson counter uses a manual reset button. Current overload and voltage level sense transformers have not yet been added to the output circuit. The dc regulator has not been connected to the inverter but has been tested with a resistive load.

b. Power Devices

Darlington power devices were compared to single transistors with integrated drive circuits. As shown in the Appendix, the Darlington offers the higher efficiency. Losses in the drive circuit of the single power device were greater than the increase in collector losses of the Darlington over the single device. Also, it is believed that the greater simplicity of Darlington over single device/driver and circuitry will ultimately result in higher reliability.

Efforts are directed toward building the power Darlington transistors by the two methods shown in Figure 2. The first process shown in Figure 2A makes use of two discrete Darlington transistor wafers mounted on two insulated collector tabs. By using the second process as shown in Figure 2B, the two Darlington pairs will be

integrated into a single silicon chip. The two transistors will be isolated by a film of silicon oxide formed by the process shown in Figure 3. A wafer design, similar to that used in building the 2N3836 Darlington transistor, has been chosen for use in both approaches.

Transistors built by both methods will be evaluated and the process yielding the best performance and highest reliability will be selected for building transistors for the breadboard and final assemblies.

The design for fabricating devices using discrete wafers is essentially complete and piece parts are on order. The preliminary design for the integrated assembly is approximately 40% complete.

c. Johnson Countdown Counter and Circuit

Tentative general specifications have been given to the integrated circuit design engineer. Each output of the Johnson counter should be capable of furnishing 2.5 ma into a Darlington power device with a total maximum and minimum V_{BE} of 2.2 and 1.1 volts, respectively. The output impedance of each flip flop should be high in order to minimize the effects of variations in the Darlington's $V_{BE's}$. Also, the Johnson counter should always lock into the proper sequence with no more than two consecutive clock pulses upon starting or recovering from some temporary malfunction.

Work during this reporting period on the single chip circuits was confined, due to a lack of manpower, to establishing circuit requirements and reviewing the initial tentative specification for the integrated circuits.

d. Power Transformers

Figure 4 shows the power transformer data. A toroidal core of rectangular hysteresis material was chosen because of its high permeability. Supermendur, (trade name of Magnetics, Inc.) the material being used, has the highest saturation flux density available (~ 21 kilogauss).

In order to insure maximum reliability, these transformers were designed so that under the worst case conditions the maximum flux level would be less than one-half of the residual flux density B_r.

e. D.C. Regulator

In order to achieve the desired efficiency, it was necessary to use a "switching"type dc regulator. The fixed frequency, variable duty cycle approach will be used for this application. The switching frequency of 4.8 KC is used since it is high enough to insure a light weight filter and yet not so high as to make switching losses appreciable. Also, a 4.8 KC signal is readily available from the countdown circuit.

Several versions of switching regulator overload control are being considered. One approach would use constant current limiting (i.e. for any overload in excess of 150% rated, output voltages would be reduced to limit the excess current). The second approach (Figure 1B and 5), which is the one presently being developed, would use simple cut-out protection. If excessive current were to flow in any leg of the three-phase output, the regulator would have its switching signal inhibited for a specific time (this inhibit time can be determined by a one-shot "ON" time). At the end of this time the switching signal would again be

applied, and as long as the overload would be present the switching regulator would be cycled in and out of the operate mode.

In the present state of the breadboard (Figure 1), two low level dc supplies are used to simulate the overload current and output voltage signals.

f. Output Filter

The three-phase output filter shown in Figure 1A was designed to have a break point at 8.5 times the fundamental as suggested by Kernick, Roof and Hernrich.[1] The result was 4% distortion at 100% load (resistive), and a no load distortion at 10%. The cores used were Magnetics Incorporated Permalloy powdered iron temperature stabilized cores.

g. Temperature Compensated Crystal Oscillator

Specifications have been submitted to two manufacturers. The frequency requested is 2.4576 mc.

[1] Kernick, A., J.L. Roof, T.M. Hernrich, "Static Inverter with Neutralization of Harmonics," AIEE Transactions (Communications & Electronics), May, 1962, pp. 59 - 68.

B. Current Problems and Proposed Corrective Action

There have been no problems encountered to date.

C. Work to be Performed During Next Monthly Reporting Period

During the next reporting interval, work will continue towards the goal of a complete fully functioning closed loop breadboard model. Considerable effort will be expended on the regulator, since its development lags behind other portions of the circuit at this time. Emphasis will also be placed on ordering commercial parts such as transformers and filter cores, ac and dc filter capacitors.

1. Power Switches

The Darlington switch shown in Figure 1A will be replaced with a 2N3836 type Darlington. This approach will bring us one step closer to the fully integrated push-pull pair. During June, the fabrication of a number of two-wafer assemblies will begin. The design of the oxide-insulated assembly will be completed during June and processing masks will be ordered so that a group of sample devices can be fabricated in July.

2. Countdown and Johnson Counter

Additional manpower is expected, which will be used to initiate a detailed investigation of the type of circuits required for this program, and on initiation of the actual circuit design effort. A desirable feature will be to use the same basic circuitry for both the Countdown array and the Johnson Counter array; thus, both circuits will come from the same slice.

3. Regulator

A differential amplifier will be required for the regulator comparison element. Most integrated circuit types require plus and minus voltages. An effort will be made to locate commercial differential amplifiers which do not require a negative voltage and/or to build one by a lead pattern change from an existing network.

Hopefully an integrated circuit version of the modified one-shot can also be obtained and tested in the circuit during the next reporting interval.

4. Three-Phase Filter

Work will continue on the filter in an effort to optimize the size and filtering capabilities. Reducing the L/C ratio and lowering the corner frequency will be considered in order to reduce the no load distortion. The presence of a small fifth harmonic content (see Appendix) makes it desirable to lower the corner frequency below 2 KC.

APPENDIX

A. Data - Preliminary Breadboard

Typical data taken with a resistive 25 Ω/phase delta load:

Input dc voltage to inverter	20.8 volts
Input dc current to inverter	5.06 amps
Peak reflected load current in collector of each transistor	1.2 amps
Output voltage (across each 25 Ω resistor)	26 V rms
Distortion of phase A-B	4.0 %
Total power output	81 watts
Power input	105 watts
Efficiency	77.1%

B. Power Switches - Darlington versus Transistor/Driver

The power switch used in this initial breadboard is shown in Figure 1. With this Darlington switch and approximately 2 ma of base drive, $V_{CE\ on}$ was never more than 1 volt with a peak reflected load current of 2.2 amps (which occurred at 150% of rated output power).

An analytical comparison was made between the Darlington switch and a single transistor/integrated circuit driver combination to determine the most efficient approach. Typical specifications were forecasted as shown below:

Darlington Specs		Transistor/Driver Specs	
$V_{CE\ on}$	= 1.4 volts	$V_{CE\ on}$	= 0.8 volts
V_{BE}	= 2 volts	V_{BE}	= 1.2 volts
I_B	= 2 ma	I_B	= 50 ma
I_C peak	= 1.2 amp (at 100% rated load)	I_C peak	= 1.2 amp (at 100% rated load)

Transistor/Driver Specs
(Continued)

V_{cc} for driver = +5 volts

I_{cc} = max current drawn from V_{cc} supply ~ 53.5 ma

Note in both instances:

I_c peak is considered to be the peak value of the positive half of a sinewave.

$V_{CE\ on}$ is considered to have a constant magnitude throughout the "ON" time.

Power losses due to switching interval are considered negligible since rise and fall times combined are assumed to be 2 μsec or less.

Darlington

Average power lost in each Darlington switch:

$$P_{avg.} = \frac{V_{BE}\ I_B}{2} + \frac{I_{c\ peak}\ V_{CE\ on}}{\pi} = \frac{(2)(2 \times 10^{-3})}{2} + \frac{(1.2)(1.4)}{\pi} = \boxed{0.735 \text{ watts}}$$

Transistor Driver

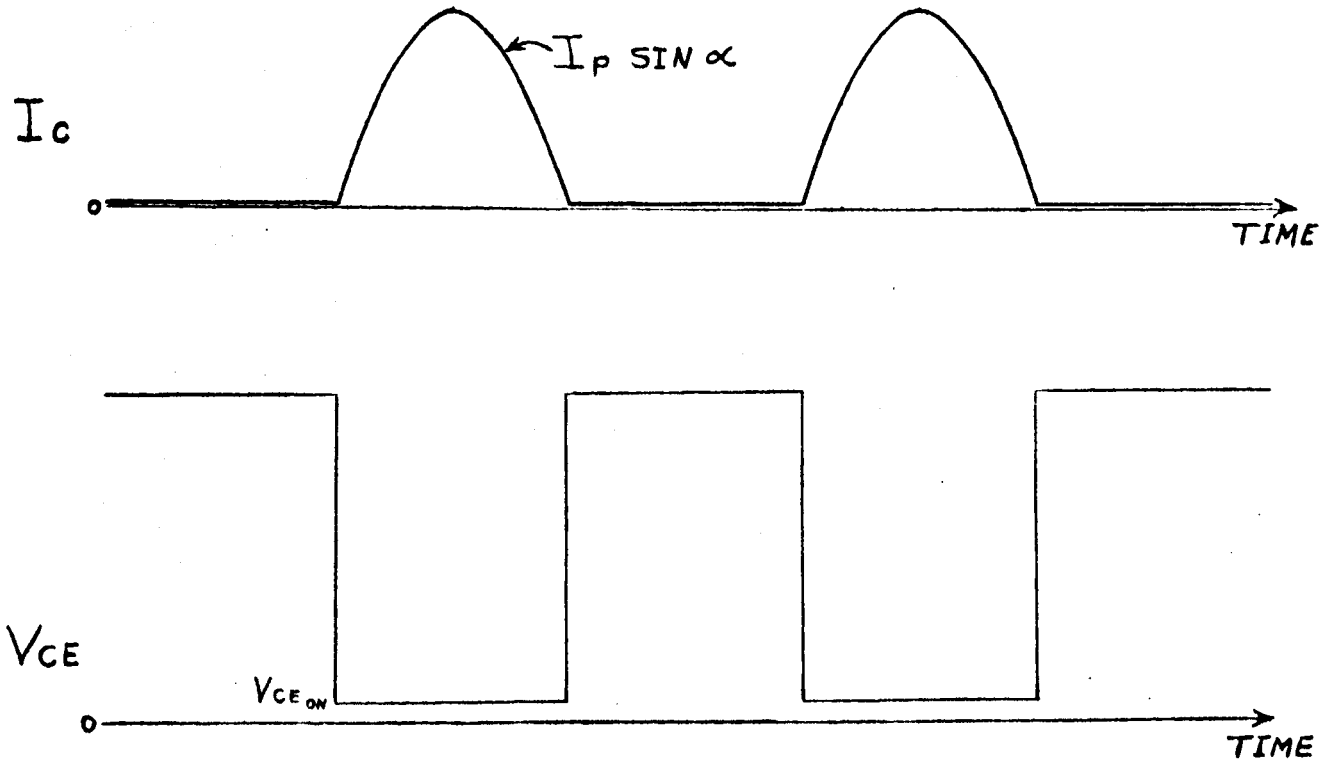
Average power lost in each transistor/driver switch = 1/12 of total power lost in all integrated circuit drivers including the common 5 volt driver power supply and all single transistor switches.

$$P_{avg.} = \frac{\left(V_{input\ DC}\ I_{cc}\right)(\text{No. of drivers on at once})}{12} +$$

$$\frac{I_{c\ peak}\ V_{CE\ on}}{\pi} = \frac{(28)\ (53.5 \times 10^{-3})\ (6)}{12} +$$

$$\frac{(1.2)(0.8)}{\pi} = \boxed{1.05 \text{ watts}}$$

Calculation of Transistor Collector Losses in the ON Condition



$$P_{lost} = \frac{1}{2\pi}\int_{0}^{2\pi} ic\ V_{CE}\ d\alpha = \frac{1}{2\pi}\int_{0}^{\pi} I_p \sin V_{CEon}\ d\alpha =$$

$$\frac{I_p\ V_{CE\ on}}{2\pi}\left[-\cos\alpha\right]_{0}^{\pi} = \boxed{\frac{I_p\ V_{CE\ on}}{\pi}}$$

C. Transformer Design

According to the latest Magnetics Inc. data on Supermendur material:

Bm minimum @ 25°C = 19K Gauss
Br minimum @ 25°C ~ (0.9) Bm minimum = 17.1K Gauss
Br minimum @ 165°C = (.955) Br minimum @ 25°C = 16.1K Gauss

Using 45% of 16.1K Gauss as the maximum permissible operating flux density Bx:

$B_x = (.45)(16.1K) = 7.25K$ Gauss .

The maximum primary voltage E, which can be transformed to the secondary was assumed to be 21 volts. (Subsequent data indicates this to be a safe conservative estimate). This voltage, and the desired max flux density B_x determine the necessary number of primary turns N_1.

$$N_1 = \frac{E\ (10^8)}{4\ B_x\ F\ A}$$

Where F = 400 cps
A = area of core in sq.cm. = 0.686

N_1 = 264 turns

The secondary turns were determined from a combination of calculations, estimations and data obtained from a first attempt.

D. Operation of Voltage Regulator (Figure 5)

This circuit is similar to the one in Figure 1B with the exception that the lab supplies have been replaced by actual sensing circuits and a differential comparator amplifier. This modification will be made in a future reporting period. This circuit operates in the following way: the voltage sense signal from the 3 ∅ output is compared to a voltage reference zener and an amplified error signal appears at the output of

the differential amplifier. This analog voltage is fed into N_1 and the output of N_1 is a constant frequency (4.8 KC) duty cycle modulated pulse train which passes through the AND gate and operates the series power switch. If an overload current is sensed, the Schmitt trigger fires and simultaneously sets the RS flip flop and activates the one-shot N_2. With the RS flip flop in a set condition and AND gate inhibits the modulated pulse train, thus shutting off the regulator. However, the RS flip flop is automatically reset when the one-shot returns to its normal state, thus enabling the AND gate to once again pass the pulse train and the regulator provides an output voltage again.

The one-shot N_1 which performs the function of an analog to variable duty cycle converter is at present built with discrete components but it is felt that with a minor lead pattern change a standard SN1005 can be used. Figure 6 shows the circuit of the SN1005 as it will be after modification and the external diodes and capacitor and resistor which will be necessary. During the "OFF" interval (i.e. when Q_1 is "ON") the capacitor C_1 charges up to $V_{cc}-V_x$ through D_1. When Q_1 is forced "OFF" C_1 charges toward V_{cc} from an initial charge of $-(V_{cc} - V_x)$ as shown in Figure 7.

Obviously the "ON" time can be varied from almost 0 to 100% duty cycle as V_x varies from V_{cc} to 0 respectively.

The Schmitt trigger shown in block form in Figure 5 is shown in schematic form in Figure 8. It uses + 3.5 volts as do all the circuits used in the switching regulator with the exception of the modified one-shot N_1. It is also anticipated that the differential amplifier, although not yet designed, will use a voltage other than 3.5 volts.

At present the series switch is made of two TIXP07 in a Darlington configuration which have been selected for good current gain and saturation voltage at 8 amps.

The output filter at present uses a 500 μf, 50 volt capacitor and an 800 μh iron core choke. Maximum ripple observed with a resistive load has been only 7 mv, despite the fact that the inductance is not large enough to maintain current flowing through it under conditions of low duty cycle operation.

Tests with the breadboard inverter indicate that the switching regulator must be capable of:

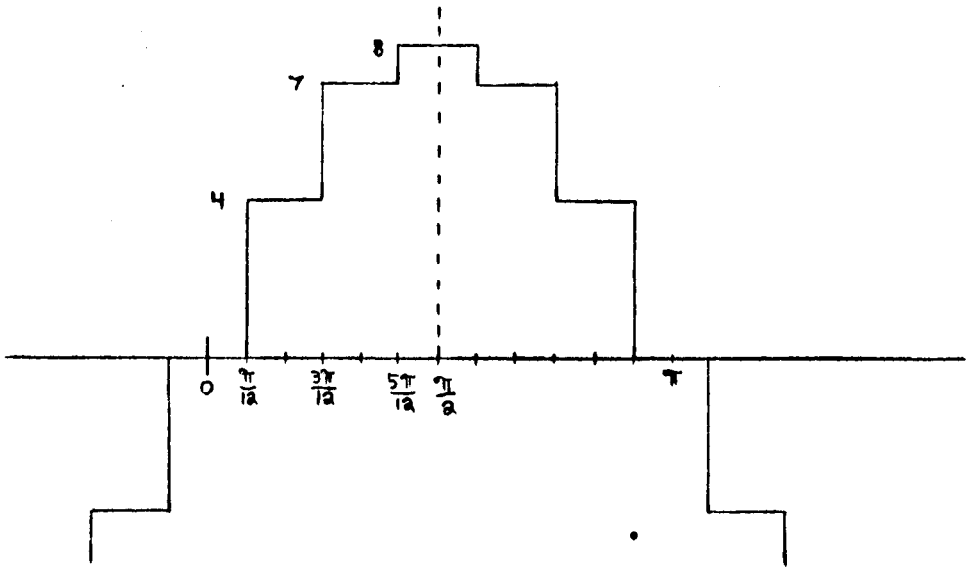
Line Supply	Regulator Output		Inverter Load % of Full Load
E_{in} Avg. Volts	E_{out} Avg. Volts	I_{out} Avg. Amps	
28	20.8	5.06	100
25	23.2	7.61	150
30	16	0.26	0

E. Filter

Filter components were calculated on the basis of a second order two element filter as shown in Figure 9A.

In a three-phase system, two inductors are in series with any phase load. Also, the capacitor across any phase has in parallel with it the series combination of the other two-phase capacitor. For this reason the filter components are altered from the calculated value as indicated in Figure 9B.

F. Waveform Analysis



$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(x)\sin nx\,dx$$

$$b_n = \frac{4}{\pi}\left[4\int_{\frac{\pi}{12}}^{\frac{3\pi}{12}} \sin nx dx + 7\int_{\frac{3\pi}{12}}^{\frac{5\pi}{12}} \sin nx dx + 8\int_{\frac{5\pi}{12}}^{\frac{\pi}{2}} \sin nx dx\right]$$

$$\boxed{b_n = \frac{4}{n\pi}\left[4\cos\frac{\pi n}{12} + 3\cos\frac{3\pi n}{12} + \frac{5\pi n}{12}\right]}$$

$$b_1 = \frac{4}{\pi}\left[4\cos\frac{\pi}{12} + 3\cos\frac{3\pi}{12} + \cos\frac{5\pi}{12}\right] =$$

$$\frac{\sqrt{2}}{\pi}\left[9 + 5\sqrt{3}\right] \sim \frac{\sqrt{2}}{\pi}\left[9+8.66\right] = \boxed{7.94}$$

$$b_3 = \frac{4}{3\pi}\left[4\cos\frac{3\pi}{12} + 3\cos\frac{9\pi}{12} + \cos\frac{15\pi}{12}\right] +$$

$$\frac{4}{3\pi}\left[\frac{4\sqrt{2} - 3\sqrt{2} - \sqrt{2}}{2}\right] = \boxed{0}$$

$$b_5 = \frac{4}{5\pi}\left[4\cos\frac{5\pi}{12} + 3\cos\frac{15\pi}{12} + \cos\frac{25\pi}{12}\right] =$$

$$\frac{4}{5\pi}\left[4\sqrt{2}\,\frac{(\sqrt{3}-1)}{4} + 3\,\frac{(-\sqrt{2})}{2} + \frac{\sqrt{2}\,(\sqrt{3}+1)}{4}\right] = \boxed{-\,0.0306}$$

$$b_7 = \frac{4}{7\pi}\left[4\cos\frac{7\pi}{12} + 3\cos\frac{21\pi}{12} + \cos\frac{35\pi}{12}\right] =$$

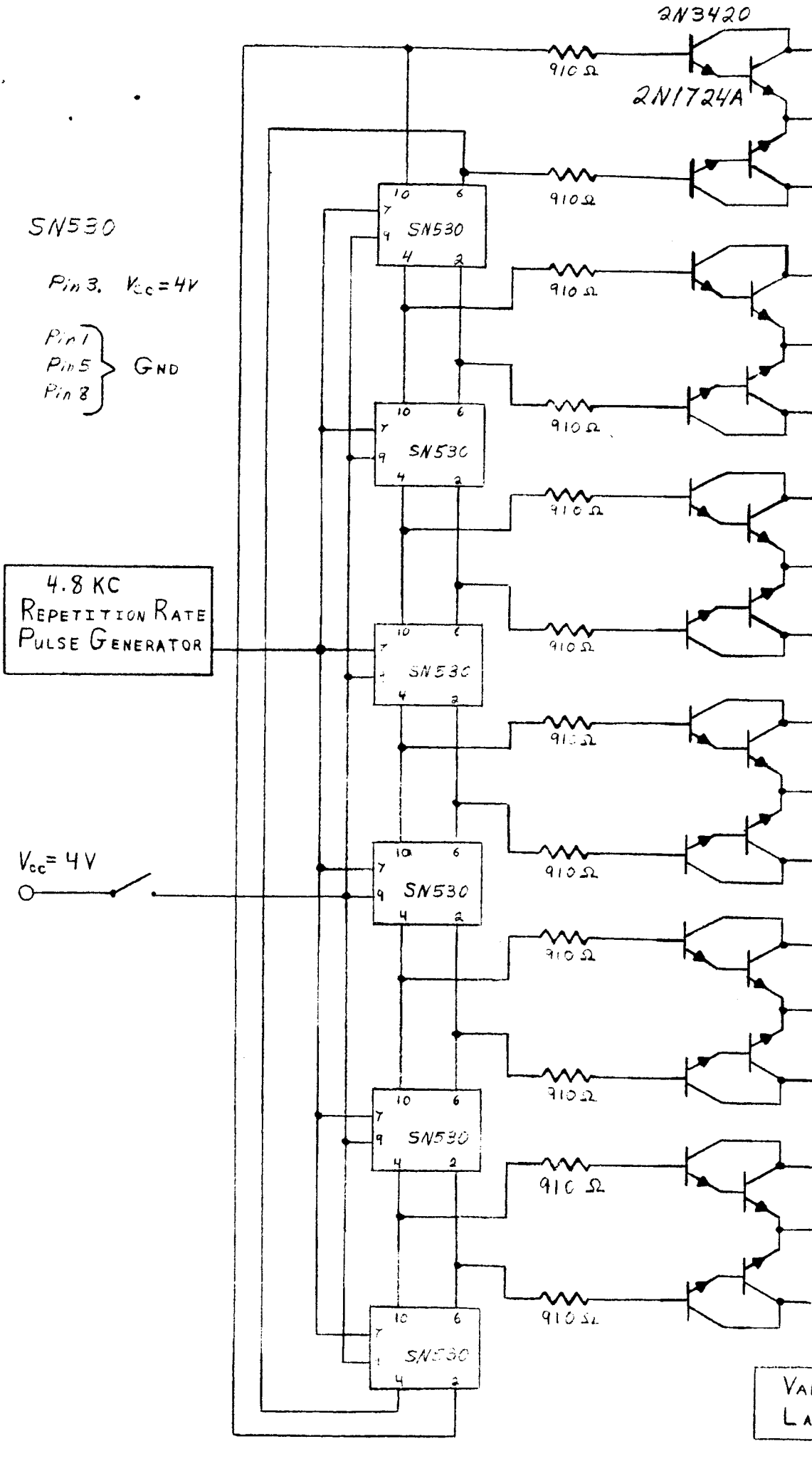
$$\frac{4}{7\pi}\left[4\sqrt{2}\,\frac{(1-\sqrt{3})}{4} + \frac{3\sqrt{2}}{2} - \frac{\sqrt{2}\,(\sqrt{3}+1)}{4}\right] = \boxed{0.0219}$$

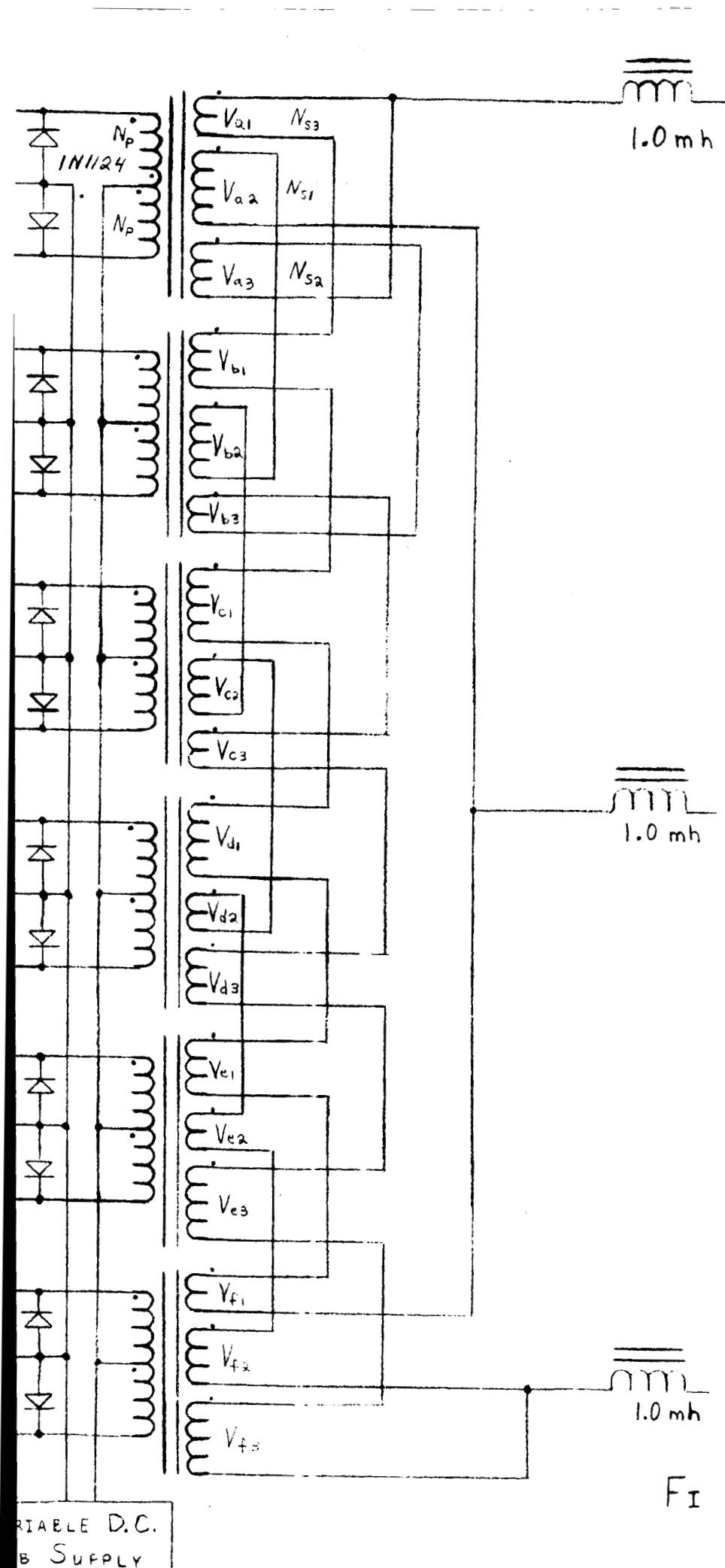
$$b_9 = \frac{4}{9\pi}\left[4\cos\frac{9\pi}{12} + 3\cos\frac{27\pi}{12} + \cos\frac{45\pi}{12}\right] =$$

$$\frac{4}{9\pi}\left[-\,4\,\frac{\sqrt{2}}{2} + 3\frac{\sqrt{2}}{2} + \frac{\sqrt{2}}{2}\right] = \boxed{0}$$

$$b_{11} = \frac{4}{11\pi}\left[4\cos\frac{11\pi}{12} + 3\cos\frac{33\pi}{12} + \cos\frac{55\pi}{12}\right] =$$

$$\frac{4}{11\pi}\left[-\,4\,\frac{\sqrt{2}\,(\sqrt{3}+1)}{4} + 3\,\left(-\frac{\sqrt{2}}{2}\right) + \frac{\sqrt{2}(1-\sqrt{3})}{4}\right] = \boxed{-\,0.722}$$


2N3420
2N1724A
910 Ω
SN530
Pin 3. V_{cc} = 4V
Pin 1
Pin 5
Pin 8
GND
4.8 KC
REPETITION RATE
PULSE GENERATOR
V_{cc} = 4V


1.0 mh
1.0 mh
1.0 mh
IN1124
N_P
N_P
V_{a1}
V_{a2}
V_{a3}
N_{S3}
N_{S1}
N_{S2}
V_{b1}
V_{b2}
V_{b3}
V_{c1}
V_{c2}
V_{c3}
V_{d1}
V_{d2}
V_{d3}
V_{e1}
V_{e2}
V_{e3}
V_{f1}
V_{f2}
V_{f3}
RIABLE D.C.
B SUPPLY

FI

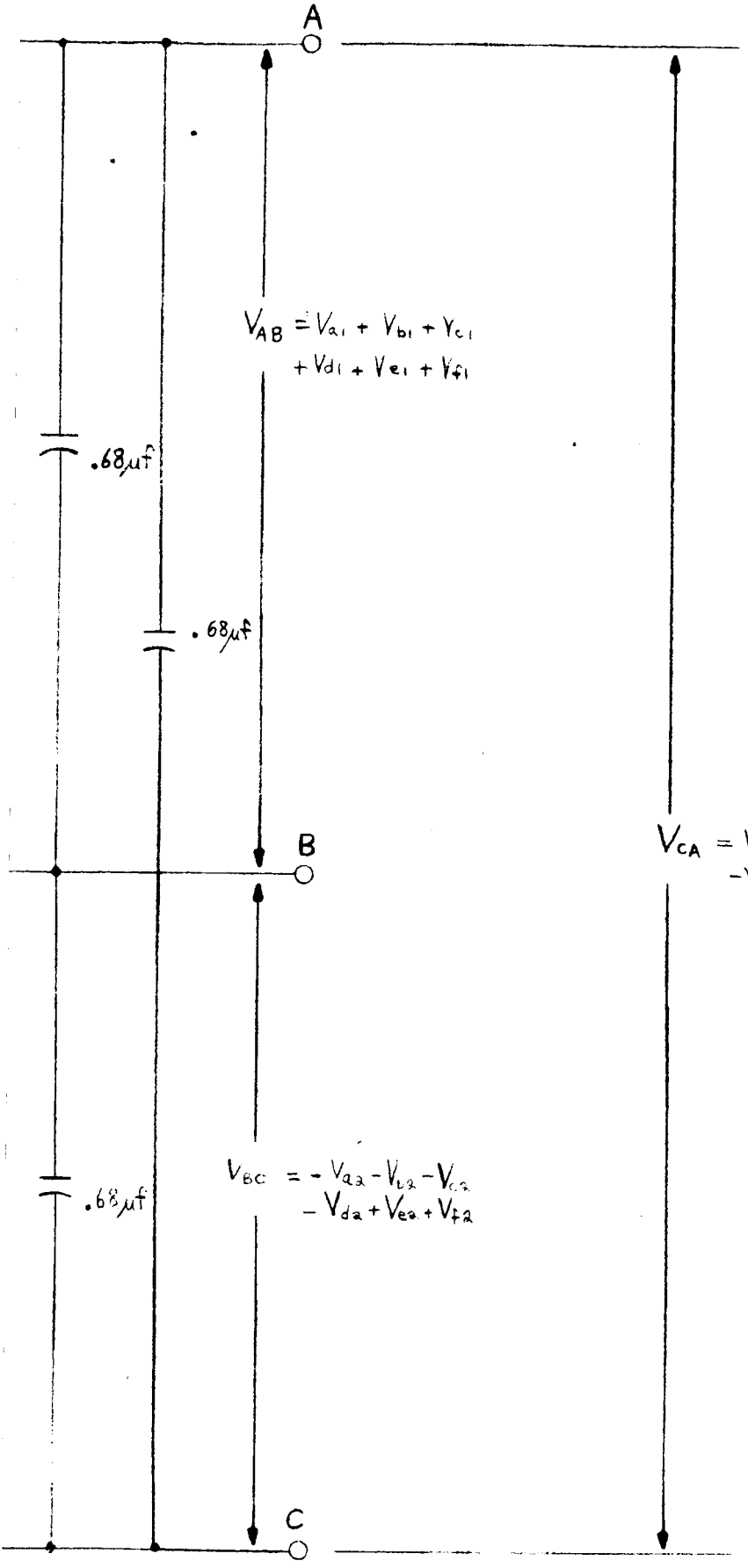
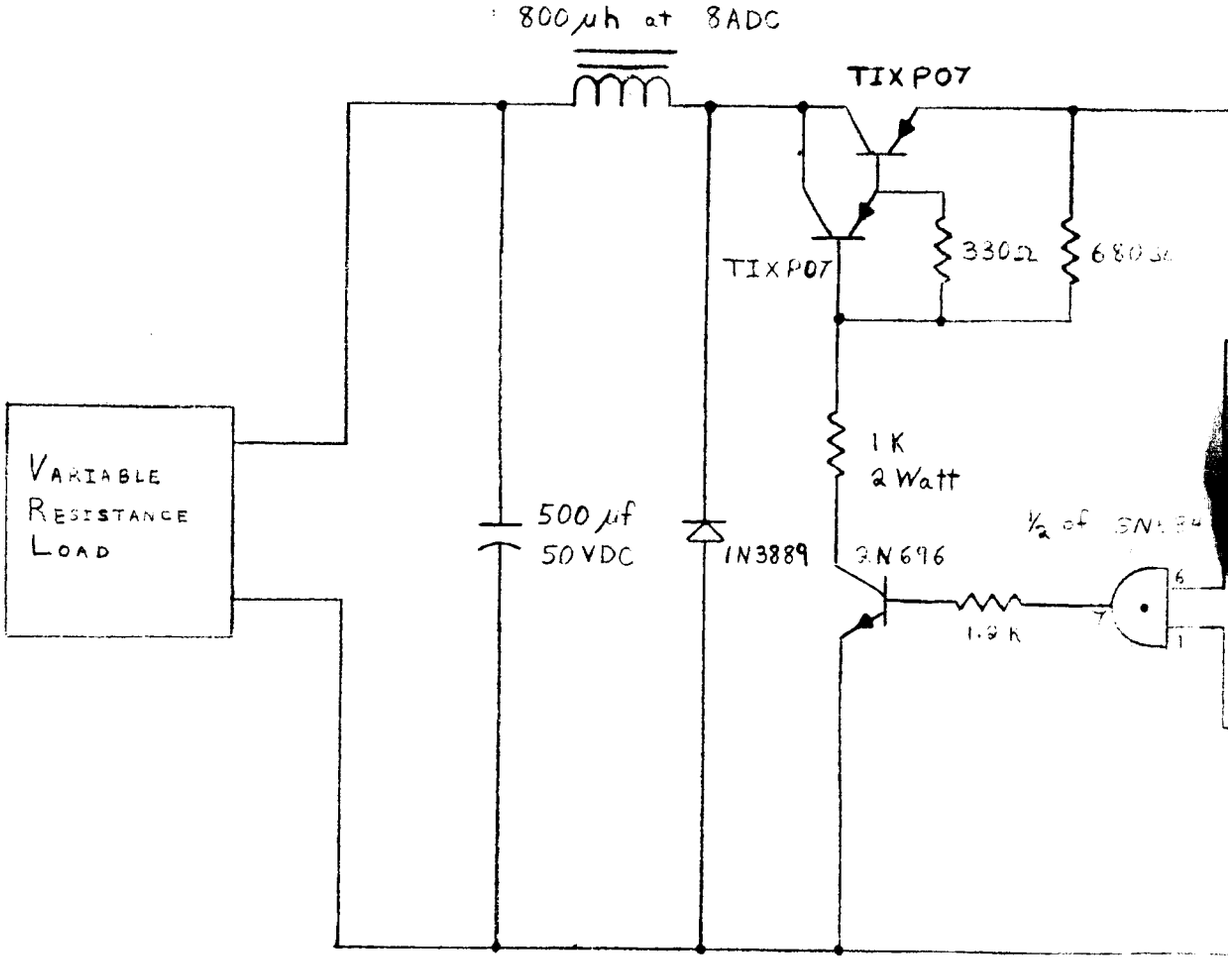
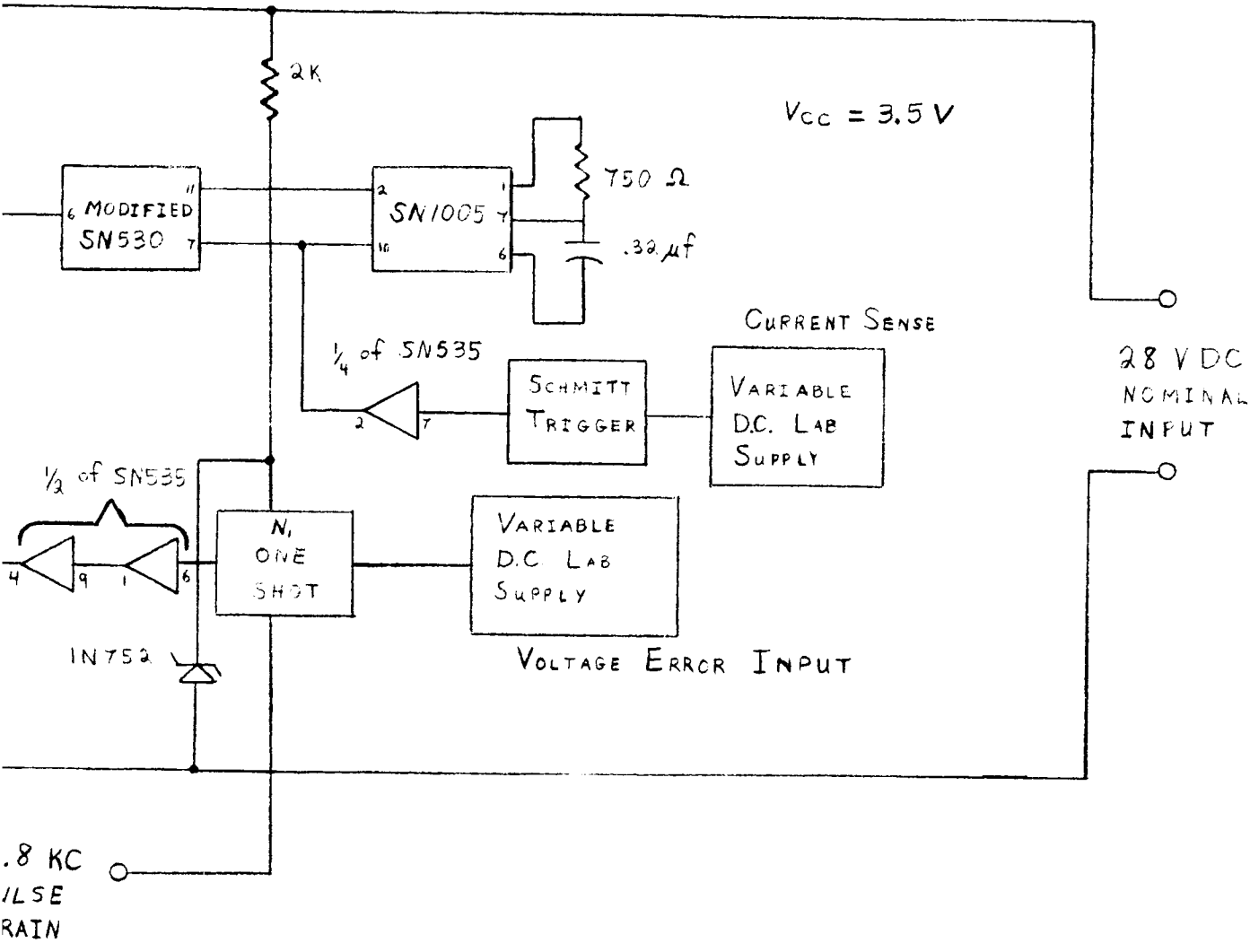

A
$V_{AB} = V_{a1} + V_{b1} + V_{c1} + V_{d1} + V_{e1} + V_{f1}$
.68μf
.68μf
B
$V_{CA} = V_{a3} + V_{b3} - V_{c3} - V_{d3} - V_{e3} - V_{f3}$
$V_{BC} = -V_{a2} - V_{b2} - V_{c2} - V_{d2} + V_{e2} + V_{f2}$
.68μf
C

FIGURE 1A


800 µh at 8ADC
TIXP07
TIXP07
330Ω
1K
2 Watt
VARIABLE
RESISTANCE
LOAD
500 µf
50 VDC
IN3889
2N696
1.8K

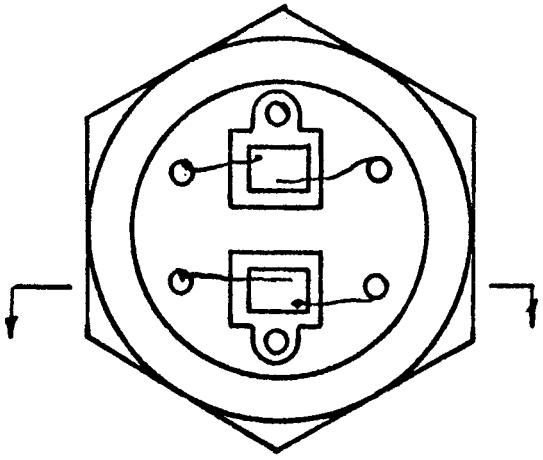


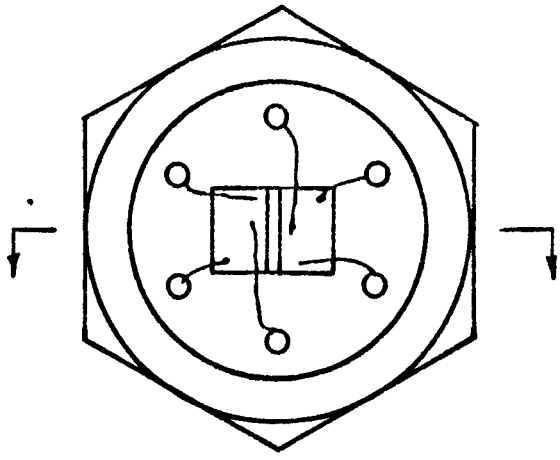
.8 KC
ILSE
RAIN

RE 1 B

PROCESS 1
TWO CHIP

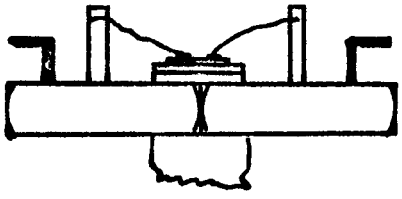
PROCESS 2
SINGLE CHIP

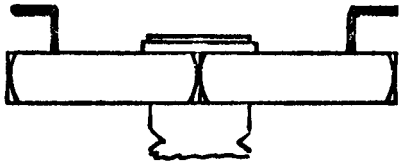




SiO_2
ISOLATION

SILICON WAFER
COLLECTOR TAB
CERAMIC INSULATION





A

B

FIGURE 2

INTEGRATED POWER TRANSISTOR FABRICATION PROCESS

1) STARTING MATERIAL
   3 - 5 Ω cm

2) ETCH ISOLATION
   GROOVES

3) DEPOSIT
   EPITAXIAL N+

4) GROW OXIDE

5) DEPOSIT
   EPITAXIAL SUPPORT

6) LAP AND POLISH
   TOP SIDE

7) DIFFUSE BASE, DIODE,
   AND EMITTER

8) APPLY CONTACTS

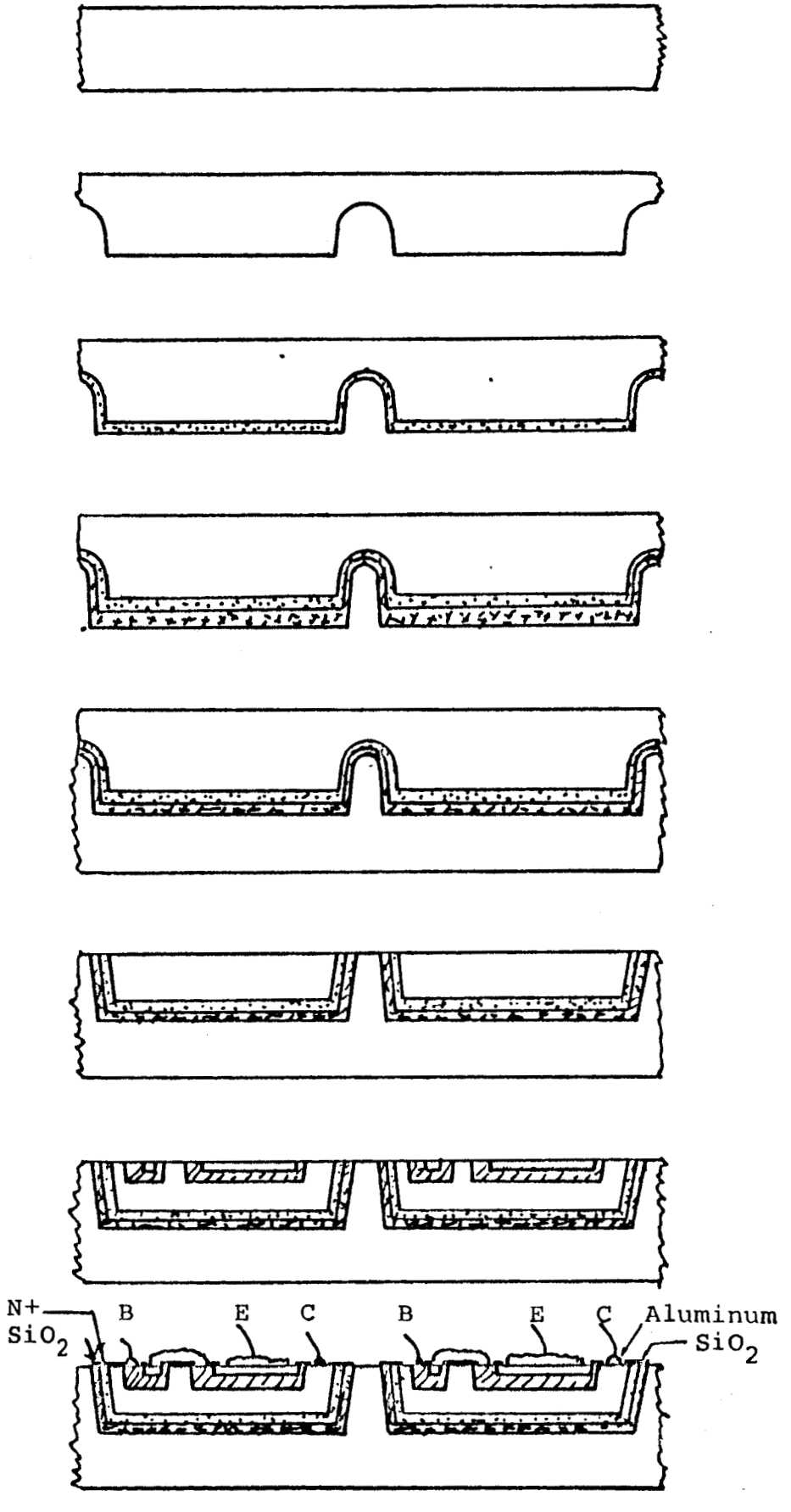
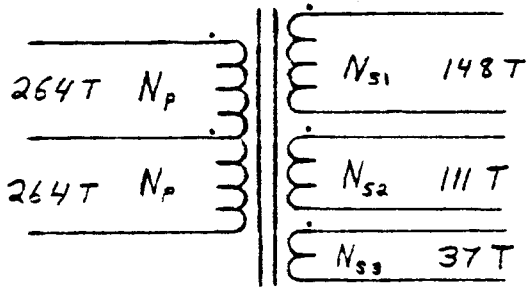


FIGURE 3

POWER TRANSFORMER



CORE - MAGNETICS 52091-2S

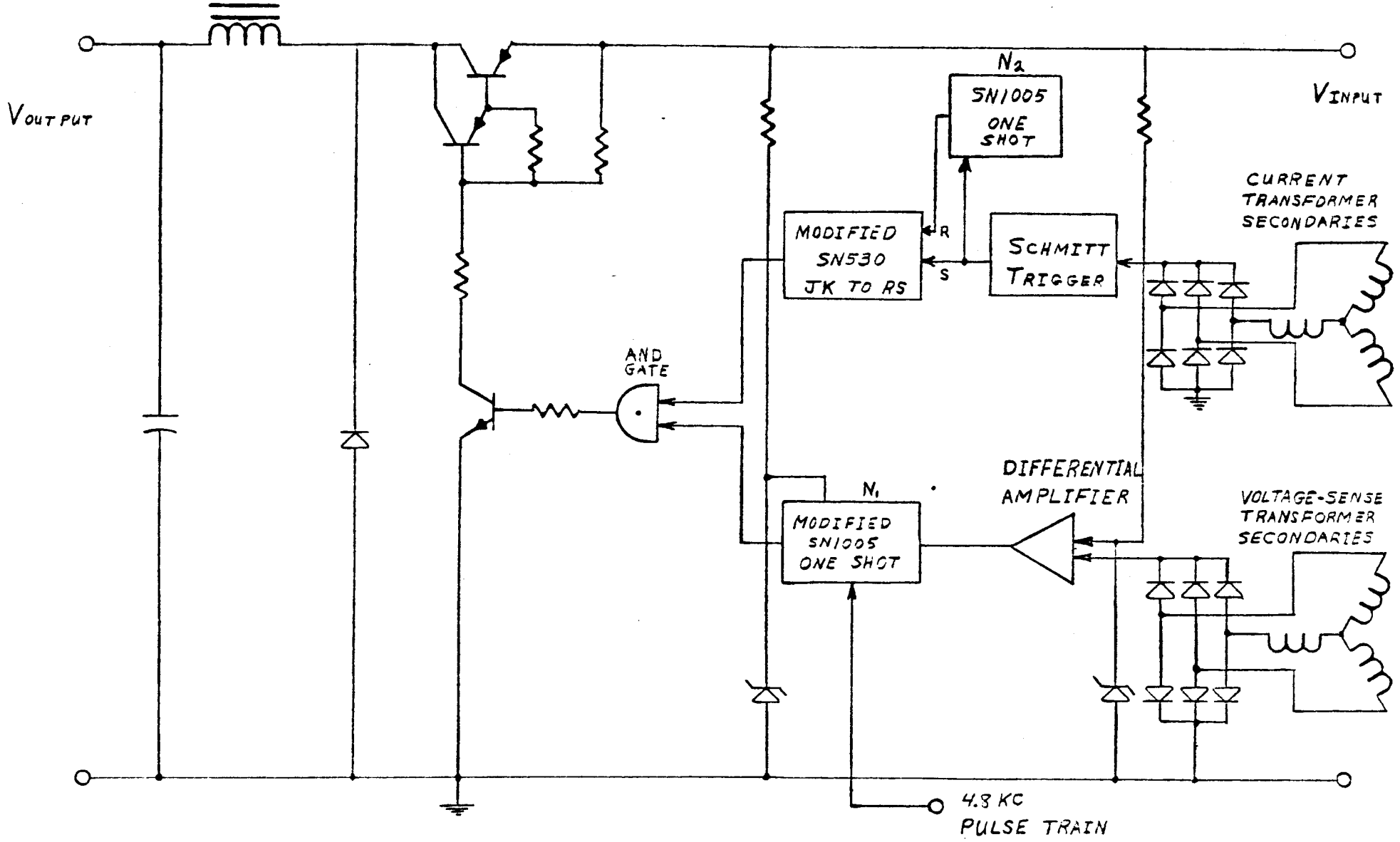
ALL WIRE = #22 HEAVY FORMVAR MAGNET WIRE

TWO PRIMARY WINDINGS ARE BIFILAR WOUND

D.C. RESISTANCE IN Ω (DATA FROM SIX TRANSFORMERS)

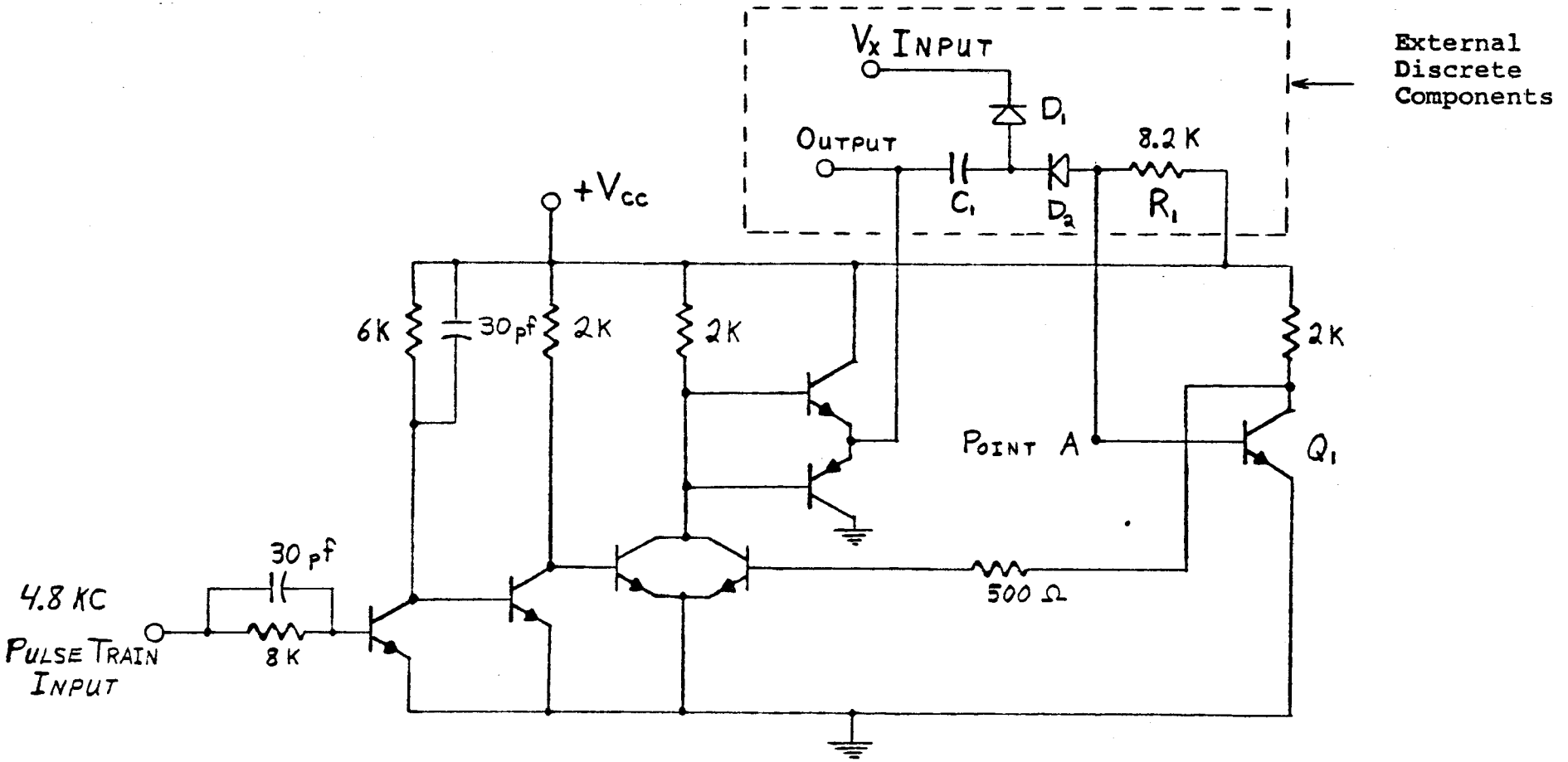
	N_P	N_{S1}	N_{S2}	N_{S3}
Max.	1.22	.77	.60	.13
Min.	.99	.65	.54	.12
Avg.	1.05	.72	.57	.127

FIGURE 4



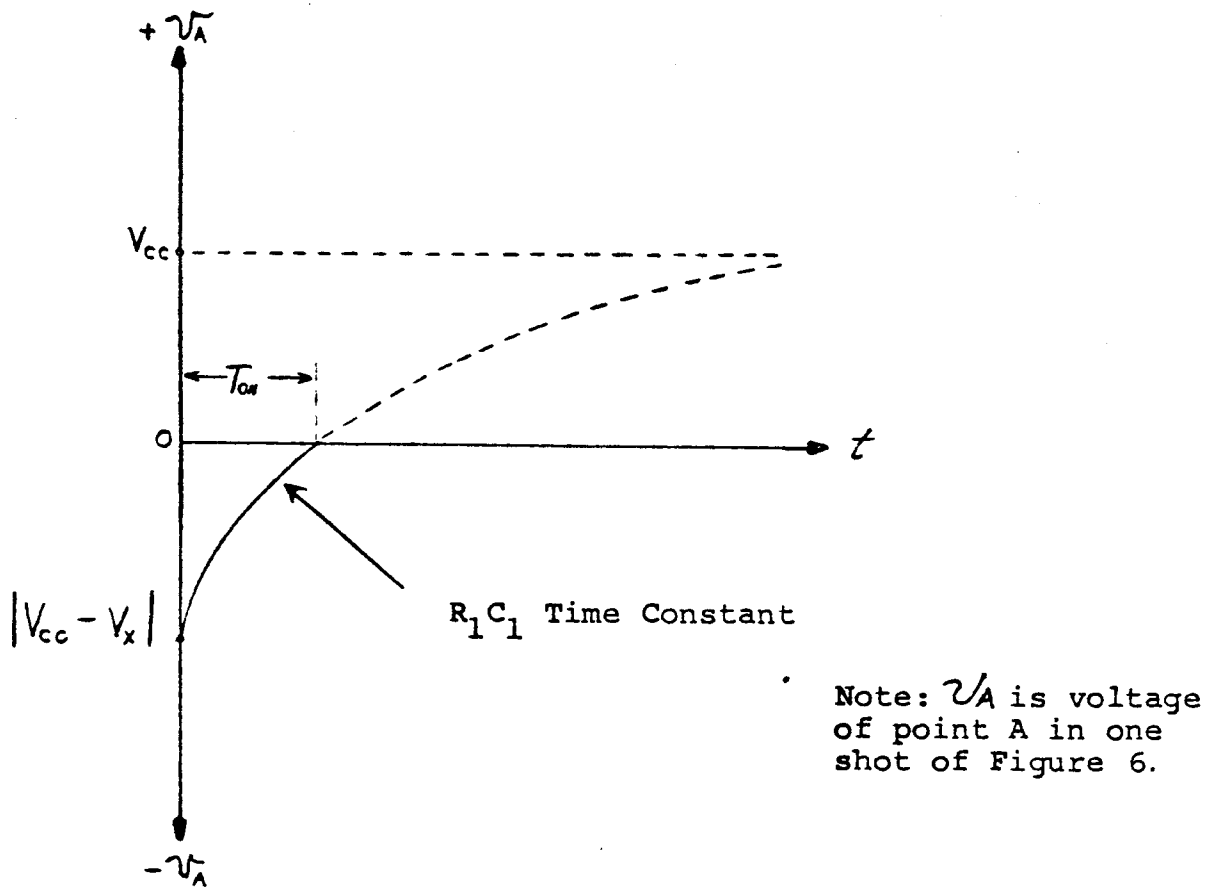
SWITCHING REGULATOR

FIGURE 5



MODIFIED SN1005 USED AS ANALOG TO VARIABLE DUTY CYCLE CONVERTER

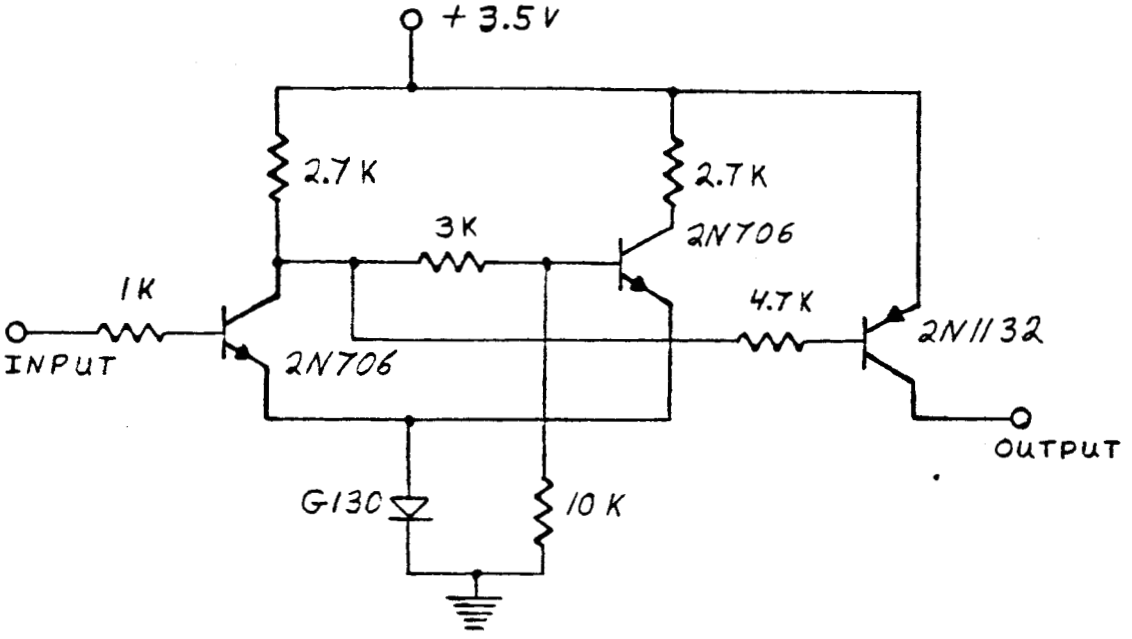
FIGURE 6



Note: v_A is voltage of point A in one shot of Figure 6.

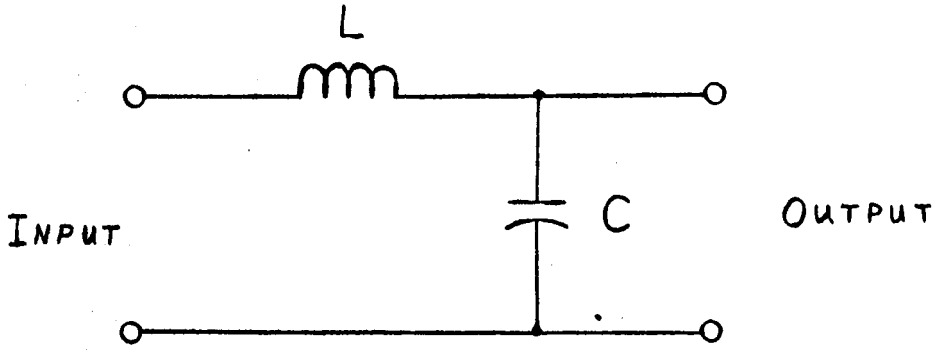
EFFECT OF V_x UPON T_{on} IN ONE SHOT OF FIGURE 6

FIGURE 7

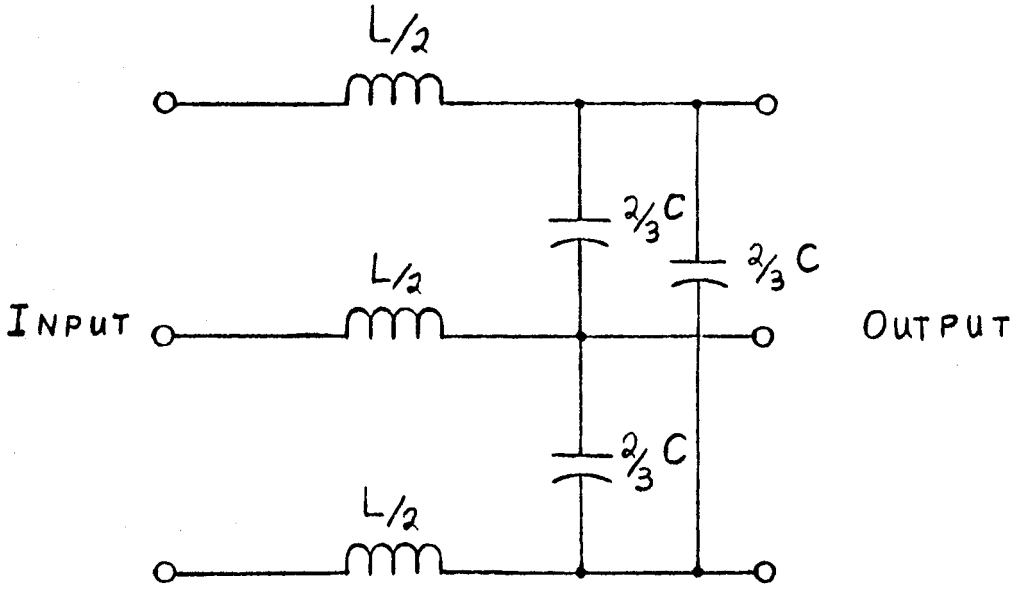


SCHMITT TRIGGER

FIGURE 8



A



B

FIGURE 9

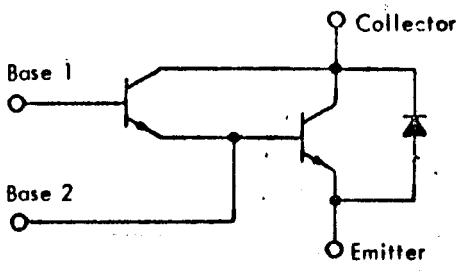
N-P-N MULTIELEMENT EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPES 2N3836, 2N3837
BULLETIN NO. DL-S 657379, MARCH 1965

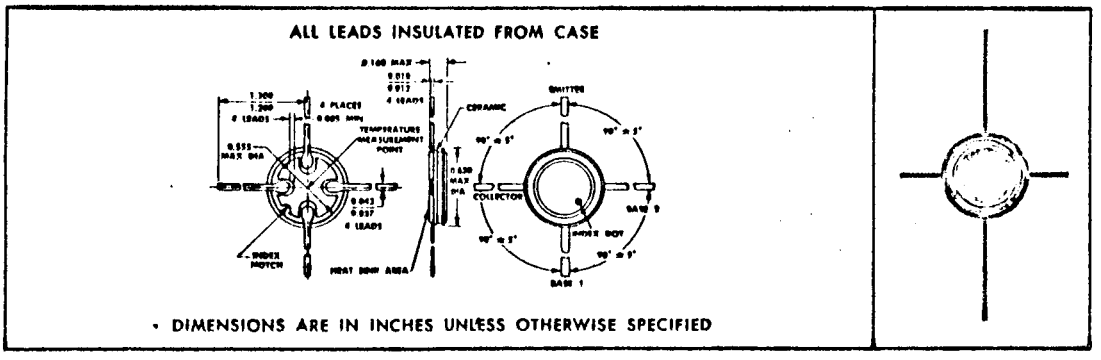
TWO TRIODES AND COMMUTATING DIODE IN MONOLITHIC DARLINGTON CONFIGURATION

- Very-High Gain — 1000 min at 5 a
- High-Speed Switching — 0.5 μsec max t_{on}

***device schematic**



***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

	2N3836	2N3837
Collector-Base-1 Voltage	80 v	100 v
Collector-Emitter Voltage (See Note 1)	60 v	80 v
Emitter-Base-1 Voltage	← 14 v →	
Collector Current	← 7 a →	
Commutating-Diode Current (See Note 2)	← −2 a →	
Base-1 Current	← 0.1 a →	
Base-2 Terminal Current	← 1 a →	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 25 w →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 w →	
Operating Case Temperature Range	−55°C to +200°C	
Storage Temperature Range	−55°C to +200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 260°C →	

NOTES: 1. This value applies when both base terminals are open circuited.

2. This applies to the total collector-terminal current when the collector is at negative potential with respect to the emitter.

3. Derate linearly to 200°C case temperature at the rate of 143 mw/C°.

4. Derate linearly to 200°C free-air temperature at the rate of 5.71 mw/C°.

*Indicates JEDEC registered data.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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TYPES 2N3836, 2N3837
N-P-N MULTIELEMENT EPITAXIAL PLANAR SILICON POWER TRANSISTORS

***electrical characteristics at 25°C case temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	2N3836		2N3837		UNIT
			MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 30 ma, I_{B1} = I_{B2} = 0, See Note 5	60		80		v
I_{CEO}	Collector Cutoff Current	V_{CE} = 50 v, I_{B1} = I_{B2} = 0		10		10	μa
I_{CES}	Collector Cutoff Current	V_{CE} = 80 v, $V_{B1\text{-}E}$ = $V_{B2\text{-}E}$ = 0		10			μa
		V_{CE} = 100 v, $V_{B1\text{-}E}$ = $V_{B2\text{-}E}$ = 0				10	
		V_{CE} = 80 v, $V_{B1\text{-}E}$ = $V_{B2\text{-}E}$ = 0, T_C = 150°C		500			
		V_{CE} = 100 v, $V_{B1\text{-}E}$ = $V_{B2\text{-}E}$ = 0, T_C = 150°C				500	
I_{EB1O}	Emitter Cutoff Current	V_{EB1} = 14 v, I_C = 0, I_{B2} = 0,		1		1	μa
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 2 v, I_C = 50 ma, I_{B2} = 0, See Note 5	1000		1000		
		V_{CE} = 2 v, I_C = 2 a, I_{B2} = 0, See Note 5	2000	20,000	2000	20,000	
		V_{CE} = 4 v, I_C = 5 a, I_{B2} = 0, See Note 5	1000		1000		
		V_{CE} = 2 v, I_C = 2 a, T_C = −55°C, I_{B2} = 0, See Note 5	500		500		
$V_{B1\text{-}E}$	Base-1 — Emitter Voltage	I_{B1} = 2 ma, I_C = 2 a, I_{B2} = 0, See Note 5	1.2	2	1.2	2	v
		I_{B1} = 10 ma, I_C = 5 a, I_{B2} = 0, See Note 5		2.6		2.6	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_{B1} = 2 ma, I_C = 2 a, I_{B2} = 0, See Note 5		1.4		1.4	v
		I_{B1} = 10 ma, I_C = 5 a, I_{B2} = 0 See Note 5		1.8		1.8	
V_{ECf}	Commutating-Diode Forward Voltage	I_C = −2 a, I_{B1} = I_{B2} = 0		1.5		1.5	v
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 v, I_C = 1 a, I_{B2} = 0, f = 20 Mc	2		2		
C_{ob1o}	Common-Base-1 Open-Circuit Output Capacitance	V_{CB1} = 10 v, I_E = 0, I_{B2} = 0, f = 100 kc		60		60	pf
C_{ob2o}	Common-Base-2 Open-Circuit Output Capacitance	V_{CB2} = 10 v, I_E = 0, I_{B1} = 0, f = 100 kc		200		200	pf

NOTE 5: These parameters must be measured using pulse techniques. PW = 300 μsec, Duty Cycle ≤ 2%.

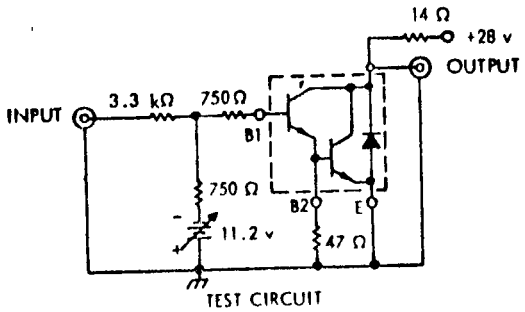
*Indicates JEDEC registered data.

***switching characteristics at 25°C case temperature**

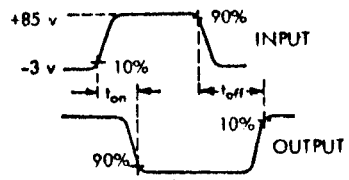
PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
t_{on}	Turn-On Time	$I_C = 2$ a, $I_{B1(1)} = 4$ ma, $I_{B1(2)} = -8$ ma,		0.5	μsec
t_{off}	Turn-Off Time	$V_{B1-E(off)} = -10$ v, $R_L = 14\ \Omega$, See Figure 1		1	μsec

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ nsec, $t_f \leq 15$ nsec, $Z_{out} = 1500\ \Omega$, PW = 5 μsec, Duty Cycle ≤ 2%.

b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ nsec, $R_{in} \geq 10$ MΩ, $C_{in} \leq 11.5$ pf.

c. Resistors must be noninductive types.

*Indicates JEDEC registered data.

TYPE TIXP07

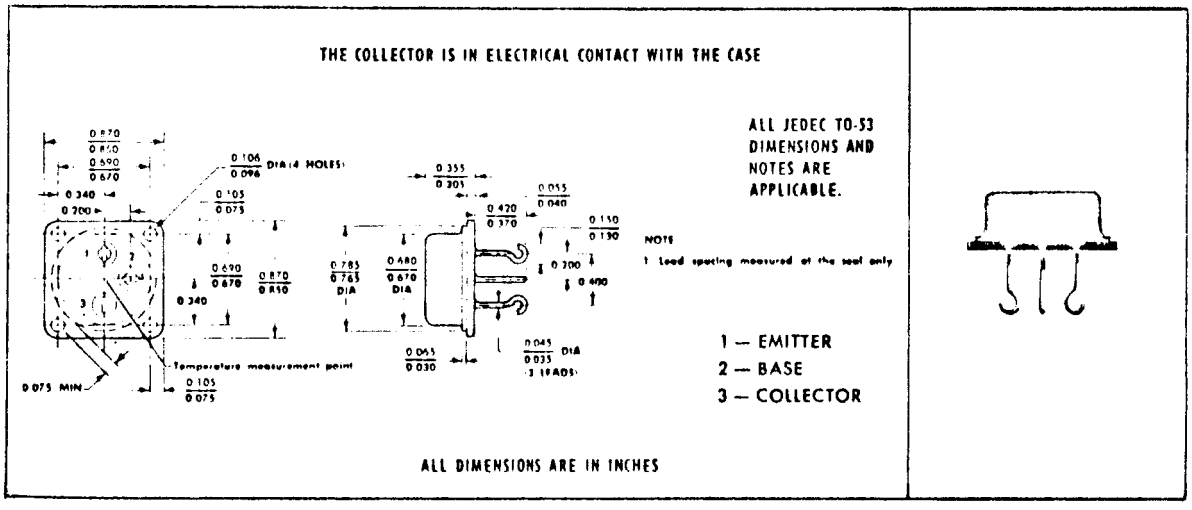
P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE TIXP07
BULLETIN NO. DL-S 657450, MARCH 1965

HIGH-VOLTAGE, HIGH-FREQUENCY POWER TRANSISTOR

- Recommended for Complementary Use With 2N1722
- 50 Watts at 100°C Case Temperature
- Maximum $r_{CE(sat)}$ of 0.25 Ohm at 5 Amperes I_C
- Maximum V_{BE} of 1.5 Volts at 5 Amperes I_C.
- Minimum f_T of 10 Megacycles

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	−100 v
Collector-Emitter Voltage (See Note 1)	−80 v
Emitter-Base Voltage	−8 v
Continuous Collector Current	−7.5 a
Continuous Base Current	−1 a
Continuous Safe Operating Region	See Figure 2
Continuous Device Dissipation at 100°C Case Temperature (See Note 2)	50 w
Continuous Device Dissipation at 25°C Free-Air Temperature (See Note 3)	3 w
Operating Case Temperature Range	−65°C to +175°C
Storage Temperature Range	−65°C to +200°C
Lead Temperature ⅛ Inch from Case for 10 Seconds	260°C

NOTES: 1. This value applies when base-emitter diode is open circuited
2. Derate linearly to 175°C case temperature at the rate of 0.67 w/C°.
3. Derate linearly to 175°C free-air temperature at the rate of 20 mw/C°.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -200$ ma,	$I_B = 0$,	See Note 4	−80		v
I_{CEO}	Collector Cutoff Current	$V_{CE} = -50$ v,	$I_B = 0$			−5	μa
I_{CES}	Collector Cutoff Current	$V_{CE} = -100$ v,	$V_{BE} = 0$ v			−1	μa
		$V_{CE} = -100$ v,	$V_{BE} = 0$ v,	$T_C = 150°C$		−100	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -7$ v,	$I_C = 0$			−0.1	μa
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -5$ v,	$I_C = -100$ ma,	See Notes 4 and 5	20		
		$V_{CE} = -5$ v,	$I_C = -2$ a,	See Notes 4 and 5	20	90	
		$V_{CE} = -5$ v,	$I_C = -2$ a,	$T_C = -55°C$, See Notes 4 and 5	12		
		$V_{CE} = -5$ v,	$I_C = -5$ a,	See Notes 4 and 5	20		
V_{BE}	Base-Emitter Voltage	$V_{CE} = -5$ v,	$I_C = -2$ a,	See Notes 4 and 5		−1.2	v
		$I_B = -500$ ma,	$I_C = -5$ a,	See Notes 4 and 5		−1.5	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -200$ ma,	$I_C = -2$ a,	See Notes 4 and 5		−0.5	v
		$I_B = -500$ ma,	$I_C = -5$ a,	See Notes 4 and 5		−1.25	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -15$ v,	$I_C = -500$ ma,	f = 5 Mc	2		
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = -15$ v,	$I_E = 0$,	f = 1 Mc		400	pf

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	1.5	C°/w
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	50	C°/w

NOTES: 4. These parameters must be measured using pulse techniques. PW = 300 μsec, Duty Cycle ≤ 1%.

5. These parameters are measured with voltage-sensing contacts located 0.25 in. from the header of the transistor. Voltage-sensing contacts are separate from current-carrying contacts.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

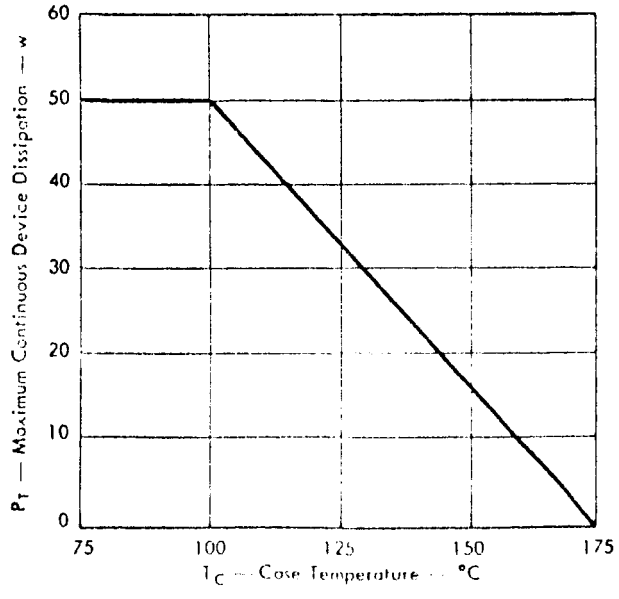

FIGURE 1

SAFE OPERATING REGION

MAXIMUM SAFE CONTINUOUS OPERATING REGION

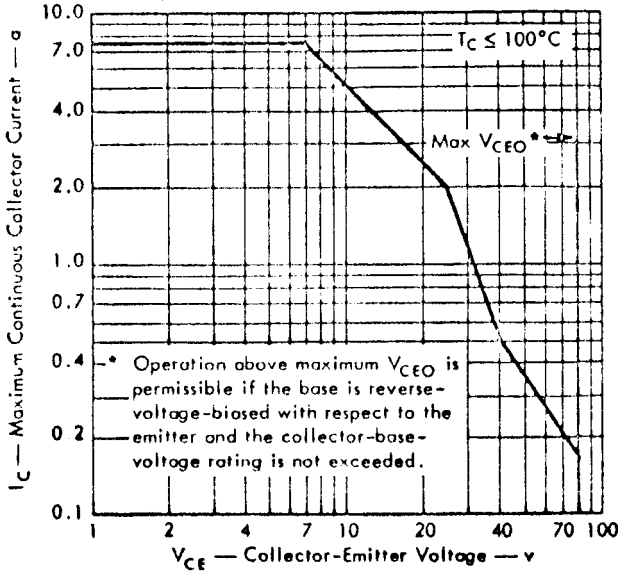

FIGURE 2

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